ABSTRACT OF THE DISCLOSURE

State retention registers for use in low-power standby modes of digital IC operation are provided, wherein: a differential circuit (M1 - M3; M1 - M4) is used to load the shadow latch from the normal functional latch; the signal (REST, RESTZ) used to restore data from the shadow latch to the normal functional latch is a "don't care" signal while the shadow latch is retaining the data during low-power standby mode; retained data from the shadow latch is restored to the normal functional latch via a transistor gate connected to a node (N10) of the shadow latch where the retained data is provided; a power supply (VDD) other than the shadow latch's power supply (VRETAIN) powers the data restore operation; and the normal functional latch is operable independently of the operational states of the high V_t transistors (M1, M2, M5 and M6; M3, M4, M5 and M6) used to implement the state retention functionality. In addition, an isolation apparatus is provided to retain an output of a logic module while the logic module is powered-down.